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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,321	09/04/2003	Richard B. Watson JR.	200301955-2 (1662-37901)	5852

22879 7590 07/22/2004

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EXAMINER	
BARBEE, MANUEL L	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,321	WATSON ET AL.	
	Examiner	Art Unit	
	Manuel L. Barbee	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,17,19,20,23,24,27,28,32-34,39-41,44,45,49,50 and 53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,17,19,20,23,24,27,28,32,39-41,44,49,50 and 53* is/are rejected.

7)☒ Claim(s) *33,34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

In paragraph 11, line 11 of the paragraph, delete "and", and insert --an--.

Appropriate correction is required.

Claim Objections

2. Claims 5 and 33 are objected to because of the following informalities:

In claim 5, line5 of the claim, "the cache clock" lacks antecedent basis.

In claim 33, line 1 of the claim, after "In", insert --a--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5, 6, 17, 19, 20, 23, 24, 45, 49 and 50 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelkar et al. (US Patent No. 5,663,991).

With regard to defining a time window between features of a first and second reference clock and comparing a plurality of cycles of a target clock with the reference clock signals to determine whether the target clock makes state transitions within the time window, as shown in claim 1, Kelkar et al. teach defining time slices with references signals each delayed by a different amount of time and measuring jitter of a

clock by determining during which time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3).

With regard to generating the first and second reference clock signals within the electronic device, phase delaying the second reference clock more than the first and defining a time window between the first and second reference clock signals, as shown in claim 2, Kelkar et al. teach using a built-in self measurement device and phase delaying the reference clock signals by different amounts to define time slices (Title, col. 3, line 62 - col. 4, line 24; Fig. 3). With regard to defining the time window between corresponding rising edges of the first and second reference signal, as shown in claim 3, Kelkar et al. teach an alternate delay device that uses inverters, which would simply delay the reference clock by a small amount and therefore windows would be between rising edges (col. 5, line 46 - col. 6, line 35; Fig. 5).

With regard to a microprocessor with a clock domain, as shown in claim 5, Kelkar et al. teach an Advanced Instruction Set Integrated Circuit (ASIC) that includes a clock (col. 1, lines 13-27). With regard to a jitter measurement circuit and measuring an uncertainty window where the cache clock makes state transitions, as shown in claim 5, Kelkar et al. teach measuring jitter and determining a time slice in which the jitter occurs (col. 3, line 62 - col. 4, line 54).

With regard to a plurality of delay units and a measurement unit, as shown in claim 6, Kelkar et al. teach a plurality of delay clock signals and comparing a clock being measured to the delayed clock signals to determine a time slice in which the jitter occurs (col. 3, line 62 - col. 5, line 2). With regard to a calibration unit, as shown in

claim 17, Kelkar et al. teach calibrating the delayed reference clock signals for measurement (col. 5, line 46 - col. 6, line 35).

With regard to generating first and second reference clock signals, defining a time window and comparing a plurality of cycle of a target clock to the reference clock signals, as shown in claim 19, Kelkar et al. teach defining time slices with references signals each delayed by a different amount of time and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition on an ASIC (col. 1, lines 13-27; col. 3, line 62 - col. 5, line 2; Fig. 3). With regard to adjusting the time window and repeating the comparing and adjusting to determine the uncertainty window, as shown in claim 19, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions, which would require repeating the comparing and adjusting (col. 6, lines 28-35).

With regard to coupling the core clock to a first and a second adjustable delay chain to created two signals delayed by different amounts, as shown in claim 20, Kelkar et al. teach using different delay on each delay element (col. 3, line 67 - col. 4, line 54; Fig. 2, 3). With regard to defining the time window between corresponding rising edges of the first and second reference signal, as shown in claim 23, Kelkar et al. teach an alternate delay device that uses inverters, which would simply delay the reference clock by a small amount and therefore windows would be between rising edges (col. 5, line 46 - col. 6, line 35; Fig. 5). With regard to adjusting the time window, as shown in claim 24,

Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions (col. 6, lines 28-35).

With regard to generating four reference clock signals, defining three time bins and comparing a plurality of target clock signals with the reference clock signals, as shown in claim 45, Kelkar et al. teach generating five clock signals that create four time slices and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3). With regard to adjusting the time window and repeating the comparing and adjusting to determine the uncertainty window, as shown in claim 45, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions, which would require repeating the comparing and adjusting (col. 6, lines 28-35).

With regard to defining the time window between corresponding rising edges of the first and second reference signal, as shown in claim 49, Kelkar et al. teach an alternate delay device that uses inverters, which would simply delay the reference clock by a small amount and therefore windows would be between rising edges (col. 5, line 46 - col. 6, line 35; Fig. 5). With regard to adjusting the time window, as shown in claim 50, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions (col. 6, lines 28-35).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 27, 28 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. in view of Neudeck (US Patent No. 5,701,335).

With regard to a measurement circuit on the die of a microprocessor and a plurality of reference clocks with different phase and comparing a target clock to the time windows created by the reference clocks, as shown in claim 27, Kelkar et al. teach defining time slices with references signals each delayed by a different amount of time and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition on a built-in self measurement (Title; col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3). Kelkar et al. do no teach a an external measurement system connected by way of a scan chain that executes software to control the measurement circuit and to adjust phase relationships of the reference clocks, as shown in claim 27. Neudeck teaches using a scan chain to control testing of integrated circuits (col. 1, lines 1-37; col. 2, lines 45-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the self measurement device, as taught by Kelkar et al., to include a scan chain for external control, as taught by Neudeck, because then components can be isolated for testing and debugging in larger systems (Neudeck; col. 1, lines 13-36).

With regard to a plurality of delay units and a measurement unit, as shown in claim 28, Kelkar et al. teach defining time slices with references signals each delayed by a different amount of time and measuring jitter of a clock by determining during which

time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3).

Kelkar et al. do not teach that the external measurement system has a microcontroller, as shown in claim 32. Neudeck teach test instructions and test data being communicated to a circuit being tested (col. 1, lines 13-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the self measurement device, as taught by Kelkar et al., to include a scan chain for external control, as taught by Neudeck, because then components can be isolated for testing and debugging in larger systems (Neudeck; col. 1, lines 13-36).

7. Claims 39, 40, 44 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al in view of Applicant's Admitted prior art.

With regard to a core region to execute software routines and determining skew and jitter, as shown in claim 39, Kelkar et al. teach measuring the jitter on an ASIC (col. 1, lines 13-27; col. 3, line 62 - col. 5, line 2). Kelkar et al. does not teach that the ASIC has cache memory, as shown in claim 39. Applicant teaches that it is rare to find a microprocessor manufacturer who does not incorporate at least some cache on the microprocessor die (Applicant's specification, par. 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the self measurement device, as taught by Kelkar et al., to include at least some cache memory, as taught by Applicant, because the size of various components on silicon substrates could be shrinked (Applicant's specification, par. 4).

With regard to a first and second reference clock and comparing a cache clock with the reference clock signals to determine skew and jitter, as shown in claim 40, Kelkar et al. teach defining time slices with references signals each delayed by a different amount of time and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3). With regard to a calibration unit, as shown in claim 17, Kelkar et al. teach calibrating the delayed reference clock signals for measurement (col. 5, line 46 - col. 6, line 35).

With regard to jitter measurement, four delay units, a measurement circuit and a calibration unit, as shown in claim 53, Kelkar et al. teach defining time slices with references signals each delayed by a different amount of time and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition and calibrating the delayed reference clock signals for measurement (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3; col. 5, line 46 - col. 6, line 35). Kelkar et al. does not teach that the ASIC has cache memory, as shown in claim 53. Applicant teaches that it is rare to find a microprocessor manufacturer who does not incorporate at least some cache on the microprocessor die (Applicant's specification, par. 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the self measurement device, as taught by Kelkar et al., to include at least some cache memory, as taught by Applicant, because the size of various components on silicon substrates could be shrinked (Applicant's specification, par. 4).

8. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. in view of Applicant's admitted prior art as applied to claims 39 and 40 above, and further in view of Neudek.

Kelkar et al. and Applicant teach all the limitations of claims 39 and 40 upon which claim 41 depends. With regard to adjustable delay means, as shown in claim 41, Kelkar et al further teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions, which would require repeating the comparing and adjusting (col. 6, lines 28-35). Kelkar et al. and Applicant's admitted prior art do not teach a control means coupled to the adjustable delay and to a scan chain to adjust the delay, as shown in claim 41. Neudeck teaches using a scan chain to control testing of integrated circuits (col. 1, lines 1-37; col. 2, lines 45-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the self measurement device combination, as taught by Kelkar et al. and Applicant's admitted prior art, to include a scan chain for external control, as taught by Neudeck, because then components can be isolated for testing and debugging in larger systems (Neudeck; col. 1, lines 13-36).

Allowable Subject Matter

9. Claims 33 and 34 would be allowable if rewritten or amended to overcome the minor objection set forth in this Office action.

10. The following is a statement of reasons for the indication of allowable subject matter: None of the prior art teach a method for calibrating a measurement circuit in a system for measuring on the die of the electronic device an uncertainty window that

includes generating a first and second calibration signal each with the same frequency but differing in phase relationship by a known time, phase locking the output of a programmable delay chain to the first calibration signal and noting the number of taps required to phase lock the first calibration signal, phase locking the output of the programmable delay chain to the second calibration signal and noting the number of programmable taps required to phase lock the second calibration signal, attributing the difference in the number of taps to the known period of time and attributing each tap to a portion of the known period of time.

Response to Arguments

11. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Smith et al. (US Patent No. 5,889,435) teach an on-chip PLL phase and jitter self-test circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Manuel L. Barbee whose telephone number is 571-272-2212. The examiner can normally be reached on Monday-Friday from 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mlb

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